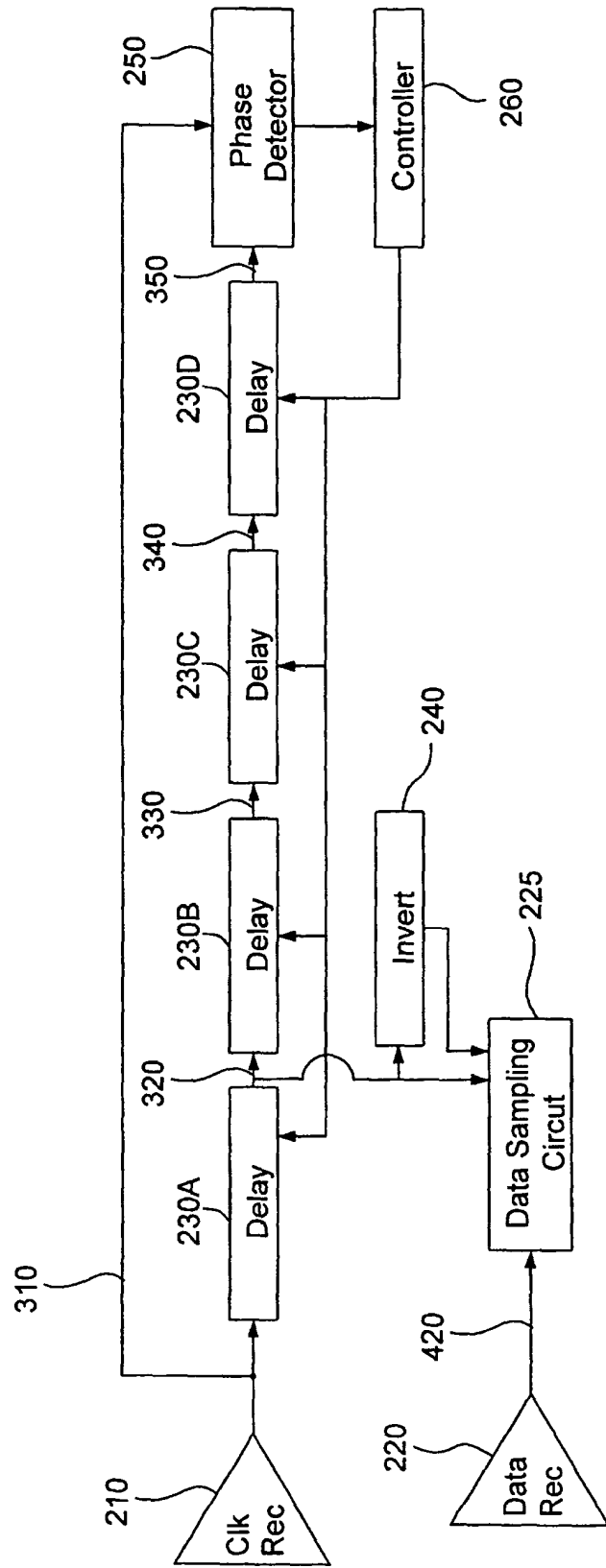
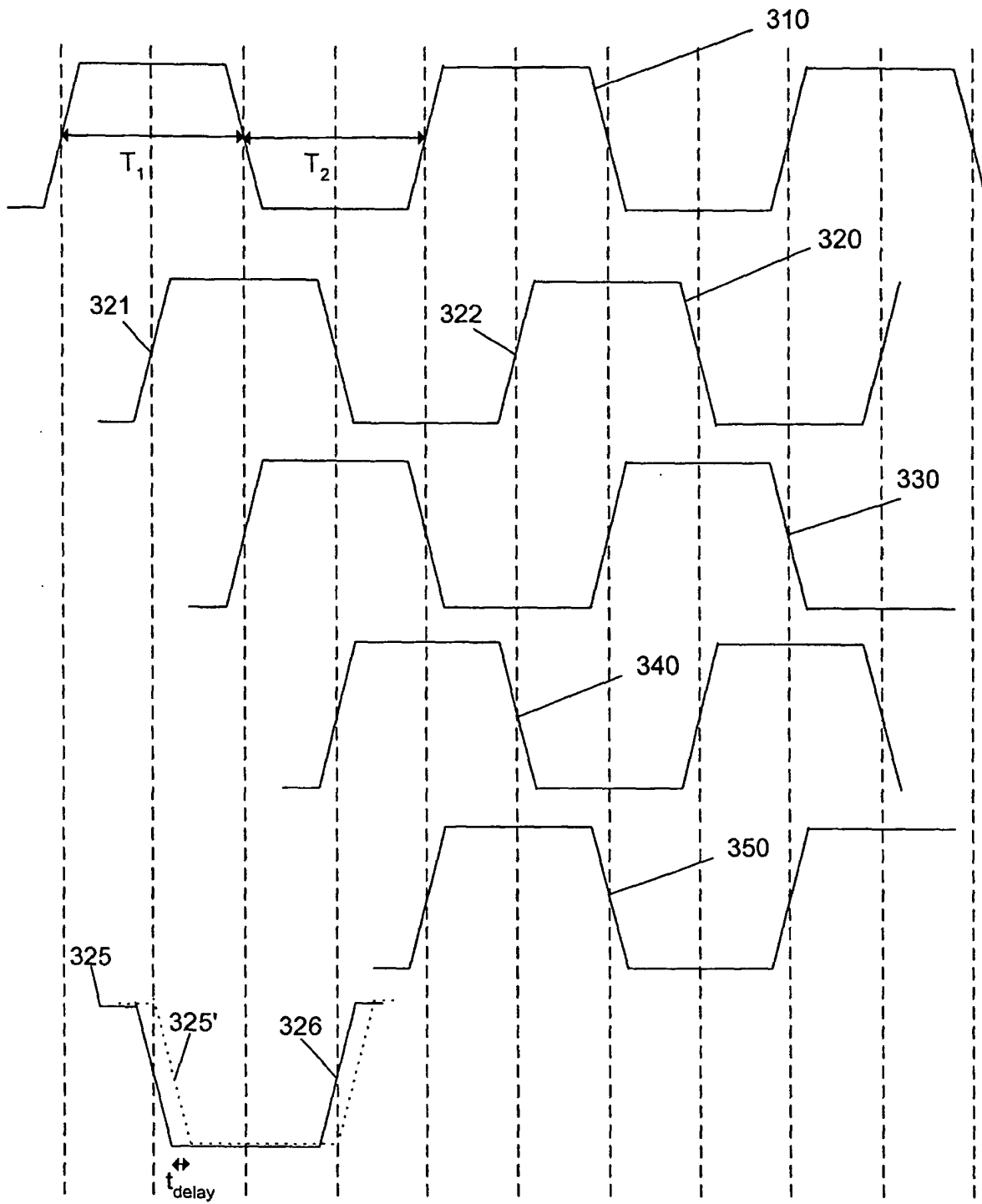


**FIG. 1**

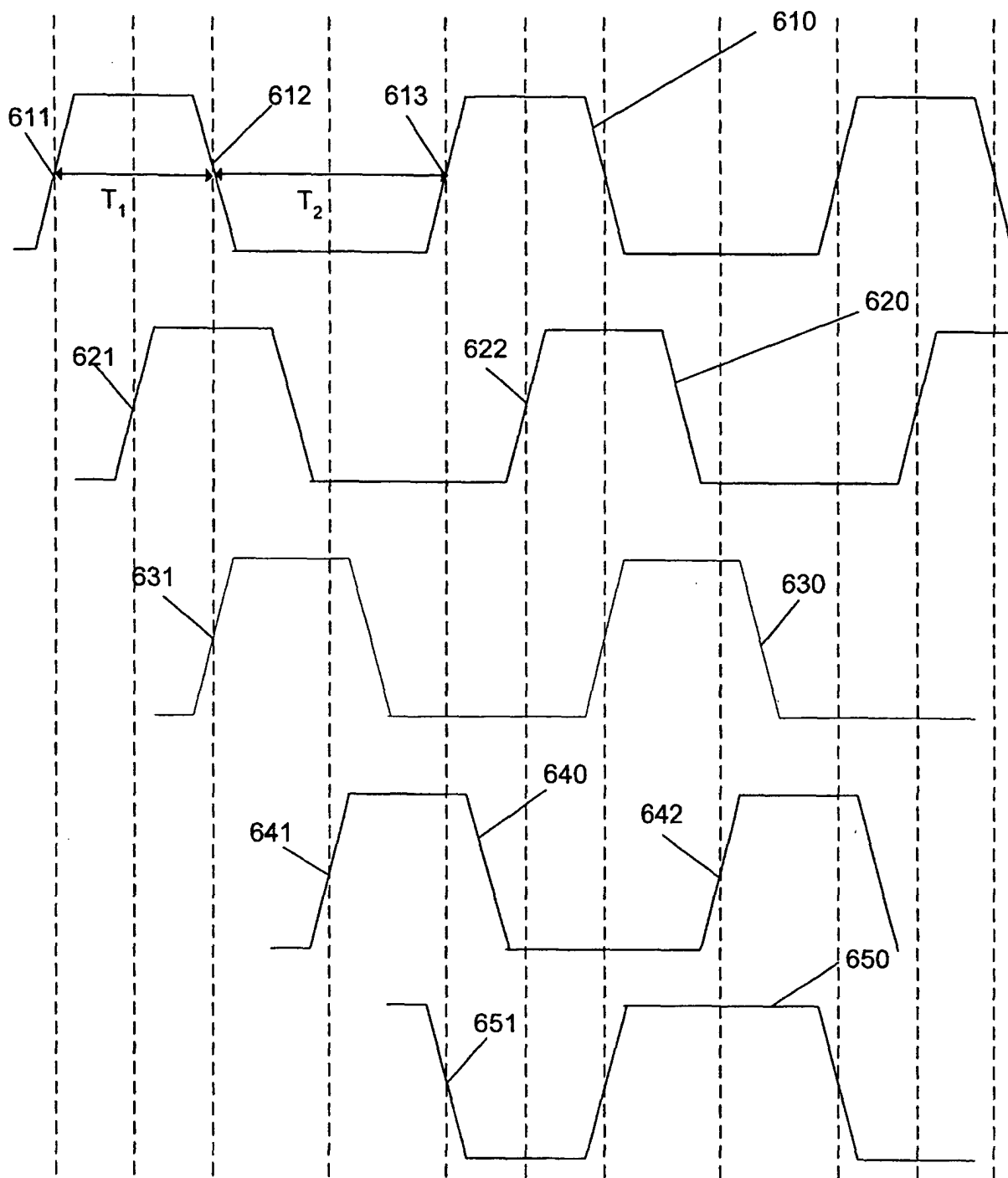
FIG. 2





**FIG. 3**

FIG. 1 is a block diagram of a multi-channel time-to-digital converter. The diagram shows two parallel processing channels. Channel 1 (top) includes a Delay Circuit (430) and a Comparator (440). Channel 2 (bottom) includes a Delay Circuit (464) and a Comparator (470). Both channels share a common Controller (450) and a Data Sampling Circuit (490). The input signal 410 is split into two paths: one path goes through a Delay Circuit (430) to a Comparator (440), and the other path goes through a Delay Circuit (464) to a Comparator (470). The output of the Comparator (440) is connected to the Controller (450). The output of the Comparator (470) is connected to the Controller (450). The Controller (450) is connected to the Delay Circuit (430) and the Delay Circuit (464). The output of the Delay Circuit (430) is connected to the Data Sampling Circuit (490). The output of the Delay Circuit (464) is connected to the Data Sampling Circuit (490). The Data Sampling Circuit (490) is connected to the input signal 420.

**FIG. 6**

**FIG. 7**

